

REMARKS

Reconsideration and allowance of this application, as amended, is respectfully requested.

This amendment is in response to the Office Action dated June 18, 2003. Appreciation is expressed for the indication of allowable subject matter in claim 9. By the present amendment, claim 9 has been redrafted into independent form to include all limitations of its parent claim 1. Accordingly, allowance of claim 9, as amended, is respectfully requested in light of the indication of allowable subject matter set forth in the Office Action.

Also by the present amendment, new claims 14-25 are presented to define the invention from a different perspective.

Briefly, the present invention is directed to a problem which the inventors have noted in thin film transistors used in the prior art in active matrix display devices. Specifically, as discussed on page 1, lines 16 et seq. and page 6, line 28 et seq., passivation films used in the past for such TFTs have fixed charges which can create an increase in the off-state current of the TFT. This can significantly deteriorate the operation of the thin film transistors, and, correspondingly, of the display device.

In order to offset this problem, Applicants have determined that forming a porous region at the upper surface of the semiconductor layer of such a thin film transistor can prevent the fixed charges in the passivation film from adversely affecting the semiconducting layer. Referring, for example, to Fig. 1, an example of a thin film transistor incorporating the present invention is shown with a gate electrode 102 formed on a glass substrate 101, a gate insulating film 103 formed over the gate electrode 102, and a silicon semiconductor layer 104 formed over the gate insulating film. In accordance with the present invention, a porous

semiconductor layer 104' is formed at the surface of the semiconductor layer 104 which adjoins the passivation film 108. In the particular embodiment of Fig. 1, discussed, for example, on page 21 et seq., the porous semiconductor layer 104' is formed of an amorphous silicon. However, other porous material could be used, if desired. Source and drain electrodes 106 and 107 and contact layers 105 are also formed over the semiconductor layer 104.

By virtue of using the porous semiconductor layer 104' at the surface of the semiconductor layer 104 which adjoins the passivation film 108, fixed charges from the passivation film 108 are prevented from increasing the off-state current in the layer 104. This is discussed, for example, in the abstract, as well as on page 9, lines 10 et seq. and page 14, line 23 et seq. Methods of forming the porous semiconductor layer 104' are discussed, for example, on page 10, line 16 et seq. and include irradiating the surface of the semiconductor layer with an ion accelerated by an electric field, the use of an anode oxidation method or the use of a self-organized resist comprised of a mixture of 2 macromolecules differing in molecular weight. Also, as defined, for example, in the dependent claims such as claims 3-5, the term "porous" can be specified in particular numeric terms such as set forth on page 10, line 4 et seq.

Reconsideration and allowance of claims 1-8 and new claim 24 over Fukunaga (USP 6,271,101) in view of Kurabayashi (USP 6,215,244) and Shor (USP 5,569,932) is respectfully requested. Independent claim 1 specifically defines the combination of features of a thin film transistor for an active matrix display device including the lamination of a semiconductor layer to a passivation film, wherein "the surface portion of the semiconductor layer on the passivation film side is porous." The dependent claims specify particular detail with regard to the porous nature of the

surface portion of the semiconductor layer. One example of this can be seen, for example, in the region 104' discussed above with regard to Fig. 1 (although claim 1 is not limited only to this specific example).

Fukunaga, on the other hand, represents a completely different structure. In particular, unlike the present invention where the porous region is provided in the final product between the semiconductor layer and the passivation film, in Fukunaga the porous silicon layer is removed and does not exist in the final product. This is clear, for example, in column 2, lines 50-53 and column 3, lines 8-12. Indeed, this is recognized in the Office Action at the bottom of page 2 which states:

"Fukunaga fails to disclose the required laminate/porous structure in the passivation structure."

In addition, it is noted in Fukunaga the porous silicon layer is formed by an anodizing treatment. The amorphous silicon used in the embodiment discussed above with regard to Fig. 1, for example, cannot be made porous by such an anodizing treatment. The feature of the surface portion of the semiconductor layer of Fig. 1 being formed of amorphous silicon is defined, for example, in newly presented dependent claim 24.

In the Office Action, the recognized shortcomings of Fukunaga are addressed in the Office Action by seeking to combining Kuribayashi and Shor with Fukunaga. However, Applicants respectfully submit that this proposed combination fails to render the claimed invention set forth in claims 1-8 and 24 obvious for a number of different reasons.

In the first place, as noted above, Fukunaga is designed specifically to remove the porous structure during the course of manufacture. As such, it would go completely contrary to the teachings of Fukunaga to leave the porous layer in place

between a semiconductor layer and a passivation layer in the final structure. In addition, in Kuribayashi, the porous silicon film which is formed for peeling a laminate of the first conductive layer, the electroluminescence film and the second electric conductive film from the crystal silicon substrate, as discussed in column 2, lines 30 et seq. As such, in Kuribayashi the porous silicon film does not remain in the peeled laminate. Instead, as noted in column 7, lines 46-50 and column 12, lines 1 and 2, the porous silicon film remaining on the transparent electrode ITO film or the reflective film 73 are removed after peeling by a mechanical polishing process. Therefore, even in Kuribayashi, the final product does not include the porous silicon film. As such, even if Kuribayashi and Fukunaga were combined, the resulting product would still not contain the porous region between the semiconductor layer and the passivation film.

Also, similar to Fukunaga, Kuribayashi forms a porous silicon film via anodization. However, as specified in claim 24, an amorphous silicon is used in one embodiment of the present invention, and this cannot be made porous by anodization. Therefore, claim 24 serves to further define over the proposed combination.

With regard to the Shor reference, this reference teaches the use of a porous silicon carbide, not a porous silicon layer such as amorphous silicon. It is not completely clear from the Office Action as to how Shor would be used in modifying Fukunaga or Kuribayashi to arrive at the final claimed laminate of a semiconductor layer, a porous surface portion of the semiconductor layer and a passivation film. In any case, even if a passivation structure from Shor were used, the problems caused by the passivation films which the present invention are directed to will not occur. As such, there is no suggestion provided by Shor for the extensive modification, indeed,

the complete redesign which would be necessary of Fukunaga and Shor to arrive at a final structure including a porous surface portion such as called for by independent claim 1 and its dependent claims 2-8 and claim 4. Therefore, reconsideration and allowance of these claims is respectfully requested.

Reconsideration and allowance of claims 10 and 11 over the combination of Zhang (USP 6,140,164) in view of Kuribayashi, Shor, and further in view of Sakaguchi (USP 6,054,363) is also respectfully requested.

Method claims 10 and 11 specifically define a method of forming a thin film transistor such as discussed above in which the surface of a semiconductor layer is made porous by an irradiating step incorporating ions, followed by forming a passivation film on the surface of the semiconductor layer after the surface has been rendered porous. It is respectfully submitted that this is completely different than the method taught by Zhang.

More specifically, in Zhang, a film is rendered porous by an anodic oxidation process, not by ion irradiation as required by claims 10 and 11. In addition, the porous film is made of aluminum rather than silicon. As such, the effect of the aluminum porous film formed by anodic oxidation in Zhang are quite different from those achieved in the present invention. Also, once again, the Office Action recognizes that the primary reference (in this case, Zhang) "fails to disclose the required laminate/porous structure, passivation structure, and the ion irradiating structure." (E.g. see page 3, paragraph 3 of the Office Action.) And, again, nothing in the cited secondary reference to Kuribayashi, Shor, or Sakaguchi would teach or suggest the complete redesign which would be necessary to arrive at the method set forth in claims 10 and 11. In particular, with the reference to Kuribayashi, as noted above, this reference teaches removing the porous film during the manufacturing

process. Thus, unlike claims 10 and 11, the final structure in Kuribayashi would not include the porous surface portion of the semiconductor layer under the passivation film, as required by claims 10 and 11. Nothing in either Shor or Sakaguchi suggests anything which would lead to modifying the teachings of Kuribayashi to further modify the teachings of Zhang to arrive at the features defined in claims 10 and 11. Therefore, reconsideration and removal of this ground of rejection is also respectfully requested.

Finally, reconsideration and allowance of claims 12 and 13 over the combination of Konuma (USP 5,747,355) In view of Kuribayashi, Shor and Sakaguchi is also respectfully requested. Konuma is essentially the same as Zhang, and, correspondingly, shares the same shortcomings noted above. In addition, in Konuma, a porous anodic film is produced, as discussed in column 3, lines 56-65, but, subsequently, this porous anodic film is removed and the top of the gate electrode is exposed (e.g. see column 3, lines 66 through column 4, line 9). As such, it is clearly not possible with the teachings of Konuma to provide a thin film transistor having a porous surface at the top of a semiconductor layer covered with the passivation film. And, again, nothing in the cited secondary references would suggest complete modification of Konuma which would be required to meet the method steps of claims 12 and 13, as discussed at length above. Therefore, reconsideration and allowance of claims 12 and 13 over these references is also respectfully requested.

Finally, reconsideration and allowance of new independent claim 14 and its dependent claims 15-23 and 25 is also respectfully requested. New independent claim 25 is similar to claim 1, but specifically defines:

"means, formed on surface portion of the semiconductor layer between the semiconductor layer and the passivation film, for

preventing fixed charges from the passivation film from entering the semiconductor layer."

Claim 15 goes on to specify that this means comprise a porous semiconductor region formed between the semiconductor layer and the passivation film. Again, this can be read on the example shown in Fig. 1, wherein a amorphous silicon region 104' is formed at the upper surface of the semiconductor layer 104 (noting that again reference to Fig. 1 is solely for purposes of example).

None of these cited secondary references discussed above or of record in this case suggest any such means formed at the surface portion of the semiconductor layer to prevent fixed charges from the passivation film from entering the semiconductor layer. Further, none of the cited references discuss that this means comprises a porous semiconductor region formed between the semiconductor layer and the passivation film. Therefore, it is respectfully submitted that newly presented claim 14 and its dependent claims 15-23 and 25 clearly define over the cited prior art, and allowance of these newly presented claims is also respectfully requested.

If the Examiner believes that there are any other points which may be clarified or otherwise disposed of either by telephone discussion or by personal interview, the Examiner is invited to contact Applicants' undersigned attorney at the number indicated below.

To the extent necessary, Applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in fees due in connection with the filing of

this paper, including extension of time fees, to the Deposit Account No. 01-2135 (Docket No. 500.40562X00), and please credit any excess fees to such Deposit Account.

Respectfully submitted,

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